Abstract of the Disclosure

A digital delay locked loop (DLL) includes a coarse delay segment and fine delay segment. The coarse delay segment includes a coarse delay range. The fine delay segment includes a fine delay range. The coarse delay segment and the fine delay segment apply a coarse delay and a fine delay to an external clock signal to generate an internal clock signal. To keep the external and internal clock signals synchronized, the DLL adjusts the fine delay or coarse delay by increasing or decreasing the fine delay or the coarse delay. The coarse delay is adjusted only when the fine delay is at a minimum or maximum delay of the fine delay range and an increase or decrease in delay is needed respectively.